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Analysis and Implementation of Efficient BLDC Motor Drive with Different Converter Systems

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Abstract

This Paper deals with analysis of efficient BLDC motor drive with various converter systems. Performance of the drive system is compared based on THD and PF at the AC mains with the following converter topology: Conventional DC-DC converter, SEPIC and CSC converter. The complete drive system is designed and modeled in MATLAB/Simulink environment for speed control over a wide range.

Keywords: BLDC, CSC, DICM, PFC, Power Quality, Sensorless Control, THD, PF, VSI.

Introduction

BLDC Motor is widely used for many low and medium power applications like fans, refrigerators, air conditioners due to its advantage of high efficiency, high torque/inertia ratio, low maintenance and wide range of speed control. A motor drive system normally consists of a power circuit, a motor and a control unit. For a BLDC motor drive, the power circuit consists of a Diode Bridge Rectifier, a DC-DC converter and a VSI . [3, 5-7].

A conventional BLDC motor drive fed by a Diode bridge rectifier results in THD of supply current of the order 60% which results in poor PF. As per IEC 61000-3-2 standard high power factor and improved power quality at the supply end is recommended [7] .Hence an efficient drive system is required to provide a wide range of speed control with power factor correction and improved power quality at the AC mains at an effective cost [1-2]

Conventional Converter Based Drive System

Conventional converters are simple Dc-dc power converters. Dc-dc converter circuits are known that can increase or decrease the magnitude of the dc voltage and/or invert its polarity.

Circuit Diagram

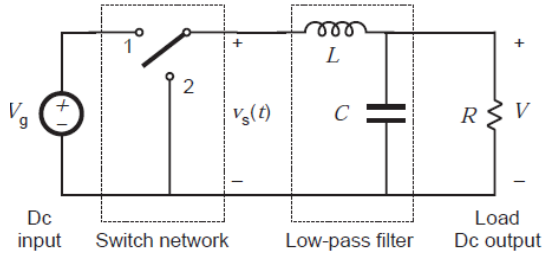

Fig.1 DC-dc Converter

Fig.1 shows basic Dc-dc buck converter circuit. When the switch is at position 1 the output voltage is equal to the input voltage. When it is at position 2 the output voltage is zero. The duty cycle of the converter switch is varied between 0 to 1. Converter switch can be a MOSFET, IGBT or Thyristor.

The average value of V_s (t) is given by

$$V_s = 1/ T_s \int_0^{Ts} V_s(t) = D V_g$$

The performance of a BLDC motor drive with a simple DC-DC converter (using a MOSFET switch) is obtained using MATLAB simulation. THD and PF are computed to quantify the performance and results are tabulated in Table I.

SEPIC Based Drive System

Single-ended primary-inductor converter (SEPIC) is a type of DC-DC converter. The SEPIC converter can step up or step down the input voltage similar to a buck-boost converter. But it differs from providing a non inverted output voltage. Output

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voltage is controlled by varying the duty cycle of the converter switch.

Basic Circuit Diagram

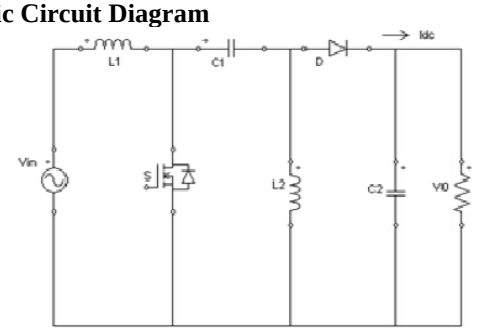

Fig.2 Circuit Diagram of SEPIC converter

Operation of SEPIC Converter

SEPIC exchanges energy between capacitors and inductors for converting output voltage from one level to another level. When MOSFET switch is turned ON, L_1 stores energy from input voltage supply and L_2 stores energy from coupling capacitor C_1. When MOSFET switch is turned OFF current through L_1 and C_1 are same. C_1 is recharged. L_1 and L_2 both deliver power to the load

The SEPIC converter is designed for power factor correction and voltage control at DC link for a VSI fed BLDC motor drive. The design equations for the output voltage, V0 of the PFC converter, input inductance L1, intermediate capacitor C1, output inductor L2 and output capacitor C2 are shown in Equations (1) – (5). D is the duty ratio.

$$V_o = V_{in}\, D / (1\text{-}D) \quad (1)$$

$$L_1 = D\, V_{in} / \{f_s\, (\Delta I_{L1})\} \quad (2)$$

$$C_1 = D\, I_{dc} / \{ f_s\, (\Delta V_{c1}) \quad (3)$$

$$L_2 = (1\text{-}D)\, V_o / \{ f_s\, (\Delta I_{L2}) \quad (4)$$

$$C_2 = I_{dc} / (2\omega\, \Delta V_{C2}) \quad (5)$$

The performance of a BLDC motor drive with a SEPIC converter is evaluated using MATLAB simulation. THD and PF are computed to quantify the performance and results are tabulated in Table I.

CSC Converter Based Drive System

In this proposed scheme Canonical Switching Cell (CSC) converter as a front End converter for PFC and Improved power quality as shown in Fig.3. PFC is achieved by the DICM operation of the CSC converter using a voltage follower approach. Two stage PFC circuits are in nominal practice in which, the former stage is used for power factor correction and the later stage for the voltage control, whereas here a single stage converter is used for both functions.

Circuit Diagram

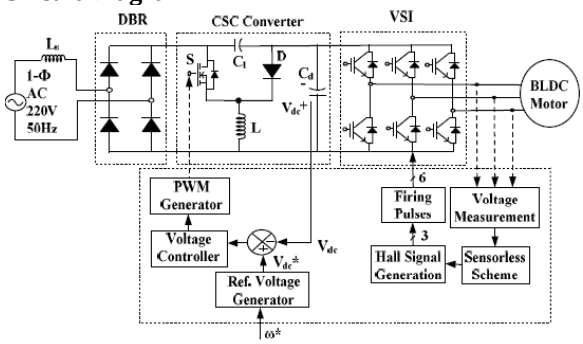

Fig.3 CSC converter fed BLDC drive

The switch of front end CSC converter is operated in high switching frequency for effective control and small size of devices like inductor; hence a high frequency MOSFET of suitable rating is used. Moreover, IGBT's (Insulated Gate Bipolar Transistors) are used in VSI with low frequency at fundamental frequency of the motor. A reference voltage corresponding to the desired speed is obtained by multiplying the reference speed with a BLDC motor's voltage constant (Kb).

Block Diagram

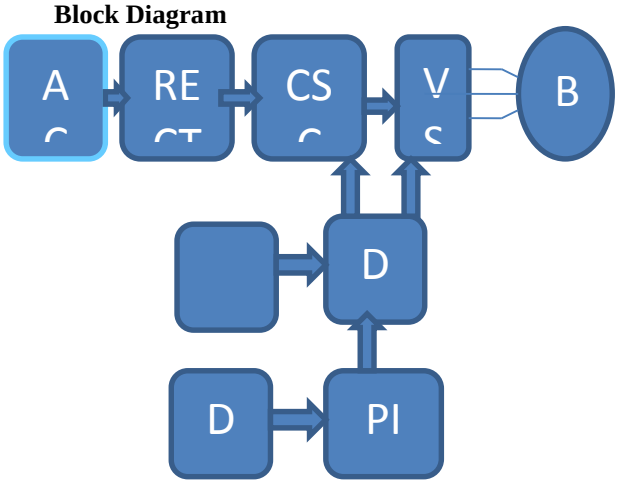

Fig.4 Block diagram of CSC converter fed BLDC drive system

This reference voltage is compared with the sensed voltage of the DC link capacitor and produces an error voltage. The error voltage is given to PI (Proportional Integral) controller to produce a controller output. Finally, a PWM signal is generated by comparing the controller output with a saw tooth wave of high frequency which is given to the MOSFET of the CSC converter for voltage control of DC bus of VSI.

Working and Operation of CSC Converter

Working of a CSC converter is similar to that of a Cuk converter but with a difference that in CSC converter transfers energy through one inductor

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compared to two inductors operation in Cuk converter. The switch and a diode operate in a complimentary fashion. When the switch is turned on, the energy stored in capacitor C1, and during the off time of the switch, it is transferred through inductor L to charge the DC link capacitor Cd. Both inductive and capacitive energy transfer takes place during this period. At the off period of switch, diode conducts to charge the capacitor C1 and only inductor is responsible for energy transfer. The energy transfer diagram of a CSC converter is shown in Fig. 5

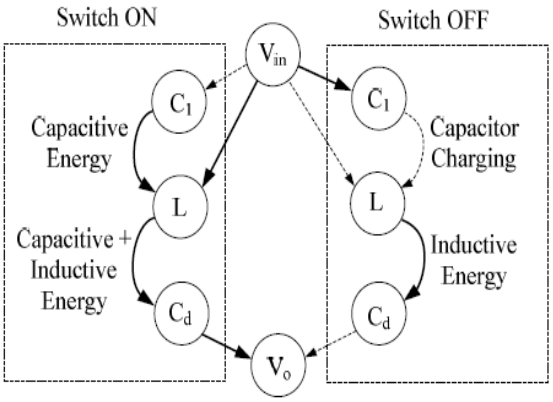

Fig.5 Energy transfer in a CSC converter

The design of a CSC is similar to a Cuk converter. The combination of a switch, diode and capacitor comprises of switching cell and is used for the design of various DC-DC converters .Fig.6 shows a CSC converter. In this, the average input voltage V_{inav}, after an uncontrolled rectifier is given as

$$V_{in(avg)} = 2V_m / \pi \quad (1)$$

where Vm is the peak voltage of the supply. The duty ratio D is given as,

$$D = V_{dc} / (V_{in(avg)} + V_{dc}) \quad (2)$$

where V_{dc} is the output voltage. The value of inductor L is to be calculated for operating in DICM. Now, when the switch S is in conduction, then the voltage at point A (shown in Fig.3.4) is applied across the inductor. Then the permitted ripple current Δi_L is given as,

$$\Delta i_L = (V_{in(avg)} + V_{C1}) D T / L \quad (3)$$

Where VC1 is the voltage across capacitor C1, and T is the switching period. Now for the critical boundary condition, $\Delta i_L = 2 I_{in}$ (4) Hence the value of critical inductance LC is calculated by putting eqn (4) in eqn (3),

$$L_C = (V_{in(avg)} + V_{C1}) D T / (2 I_{in}) \quad (5)$$

For attaining a deep DICM condition (for obtaining a DICM at worst condition i.e. lowest duty ratio), $L < L_C / 10$ (6)

The capacitor C1, in continuous mode of operation and for a voltage ripple of ΔVC1 across the capacitor, is given as [9],

$$C_1 = V_o D T / (\Delta V_{C1} R) \quad (7)$$

The value of DC link capacitor C_d is expressed as [9],

$$C_d = I_o / (2\omega \Delta V_{dc}) \quad (8)$$

where $\omega = 2\pi f_L$, f_L is the line frequency and ΔV_{dc} is the permitted ripple in DC link voltage.

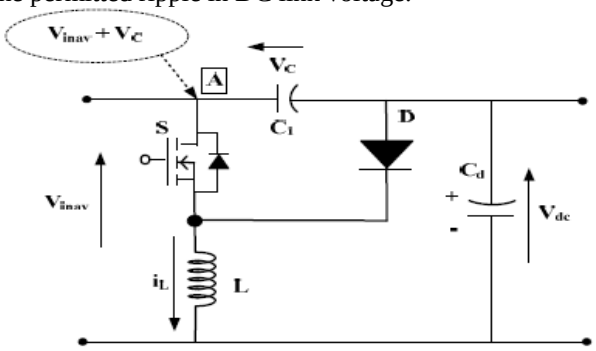

Fig.6 CSC converter

Reference Voltage Generator

The desired reference speed of BLDC motor is achieved by means of reference voltage generator. The reference voltage is obtained multiplying the speed with voltage constant K_b.

Speed Controller

DC link capacitor voltage (V_{dc}) is measured and it is compared with the reference voltage (V_r). The error voltage generated is given to PI speed controller block to produce controlled output voltage.

PWM Generator

PWM generator compares the controller output voltage with its reference voltage signal. Reference voltage is generally a saw-tooth waveform with high frequency. Whenever the controller output voltage is greater than the reference voltage the MOSFET switch is turned ON else it is turned OFF.

Controlling of BLDC Motor Drive Fed by a VSI

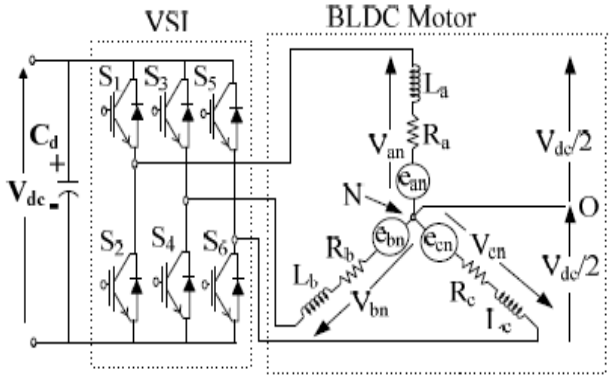

Fig.7 Equivalent circuit of a BLDC motor drive fed by a VSI

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The speed of the BLDC motor is controlled by means of DC link Capacitor voltage $V_{dc.}$ Reference potential is shown at the midpoint of DC link (O) in Fig.7. The output of the VSI for phase 'a' is given as,

$V_{ao}=V_{dc}/2$forS1=1; (11)

$V_{ao}=-V_{dc}/2$forS2=1; (12)

$V_{ao}=0$forS1=0,S2=0; (13)

where V_{dc} is the DC link voltage and the values for S1 and S2 as 1 and 0 represent the on and off condition of the IGBT's S1 and S2. When switch S1 and S4 are on then phase 'a' and 'b' are connected and the current i_a ($i_a = i_b$) flows through the motor windings and the third phase 'c' remains in floating condition as shown in Fig. 7. The equation for line voltage V_{ab} is given as,

$V_{ab}=V_{dc}=R_a+L_a\, di_a/dt+e_{an}+R_b+L_b\, di_b/dt+e_{bn}$ (14)

If $L_a=L_b=L$, $R_a=R_b=R$, $i_a=i_b$ and $e_{ab}=e_a+e_b$ then,

$V_{dc} = 2\,R\,i_a + 2\,L\,di_a/dt + e_{ab}$ (15)

Where i_a is the line current (or the phase current) of the motor. Similarly the other combination of switches can be obtained.

Simulation Results

Simulation Results for Conventional Converter Fed BLDC Drive

Simulation Parameters:

Input supply voltage: 220V
Supply Frequency : 60HZ
MOSFET Resistance: 0.1 ohm

Stator Current

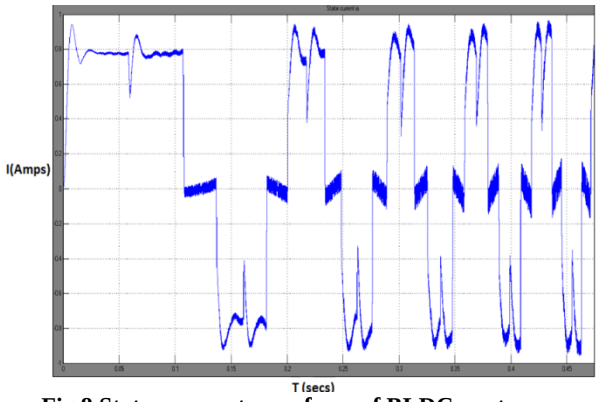

Fig.8 Stator current waveform of BLDC motor

Speed

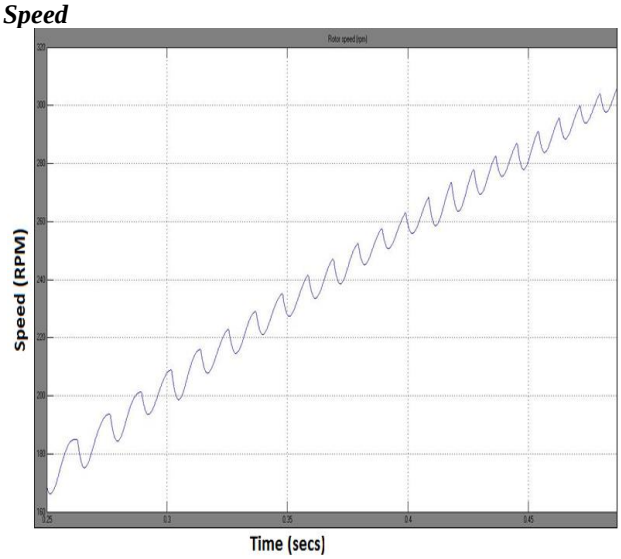

Fig.9 Speed response of BLDC motor

Torque

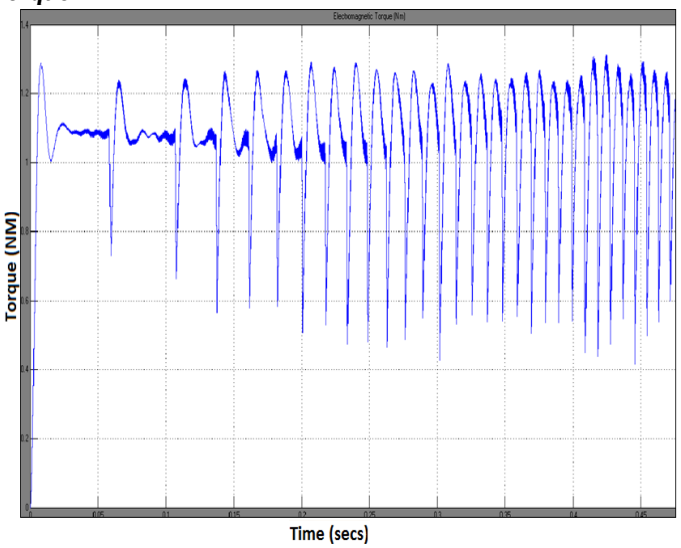

Fig.10 Torque waveform of BLDC motor

Simulation Results for SEPIC Fed BLDC motor

Simulation Parameters:

- Input supply voltage: 220V
- Supply Frequency : 60HZ

SEPIC converter

- MOSFET Resistance: 0.1 ohm
- Inductance L1 : 1 H
- Inductance L2 : 10 mH
- Capacitor C1, C2: 5 uF
- Diode Resistance: 0.001 ohm

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Stator Current

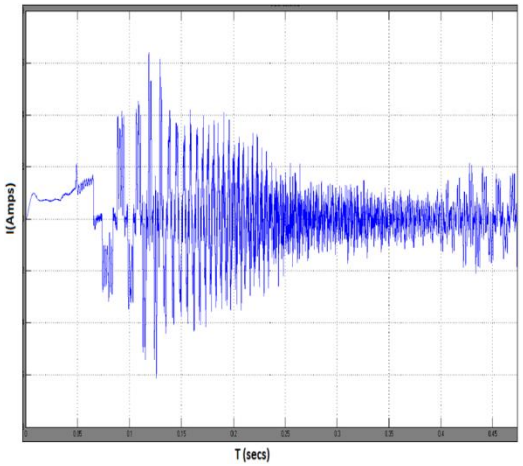

Fig.11 Stator Current waveform for BLDC motor

Speed

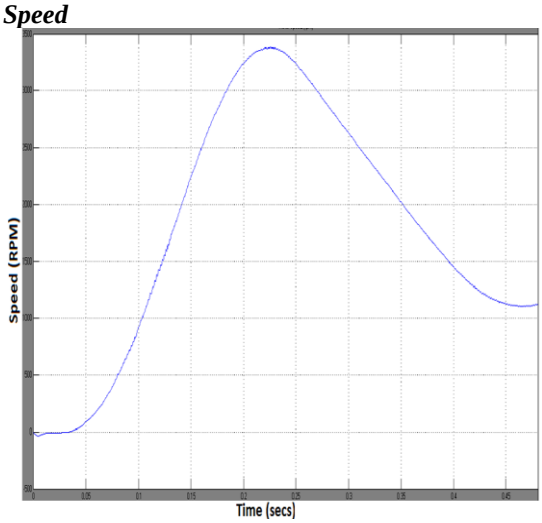

Fig.12 Speed response of BLDC motor

Torque

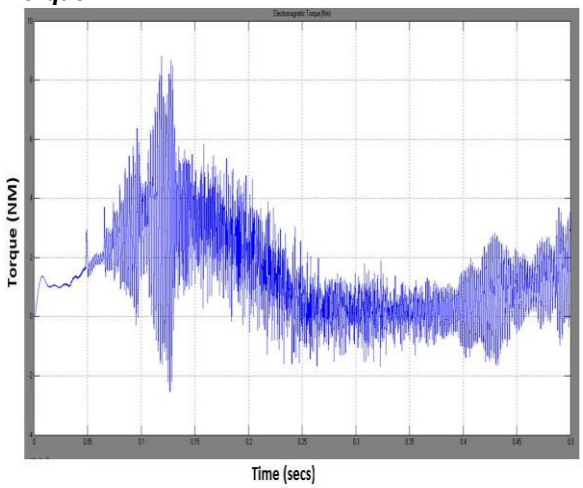

Fig.13 Torque waveform of BLDC motor

Simulation Results for CSC Converter Fed Drive

Simulation Parameters:

Input supply voltage: 220V
Supply Frequency : 60HZ

CSC Converter:

MOSFET Resistance: 0.1 ohm
Inductance: 170 uH
DC link capacitor : 15000 uF
Reference value : 250
PWM Generator Carrier Freq: 45 KHZ

Stator Current

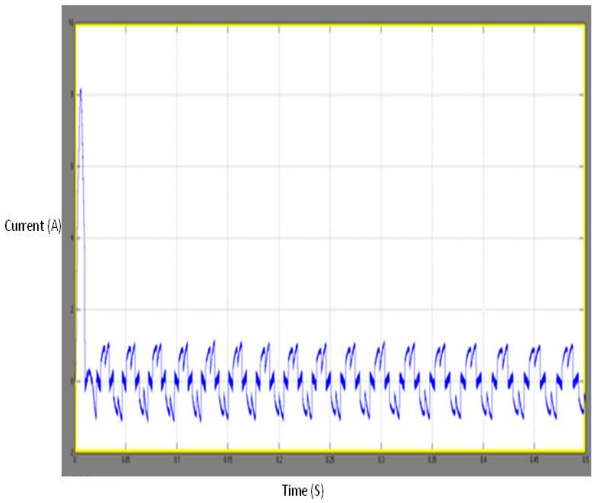

Fig.14 Stator Current waveform for BLDC motor

Speed

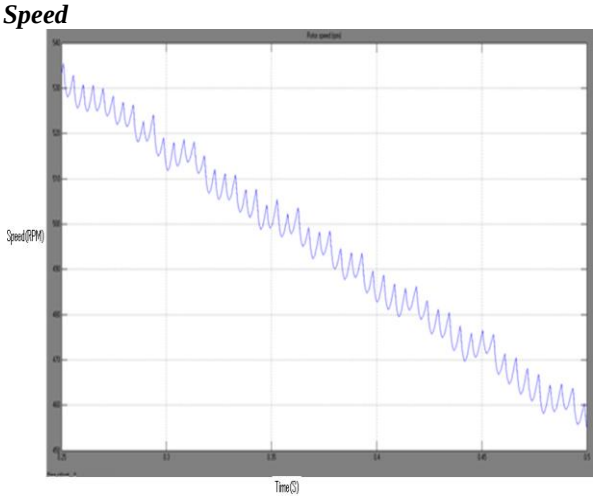

Fig.15 Speed response of BLDC motor

Torque

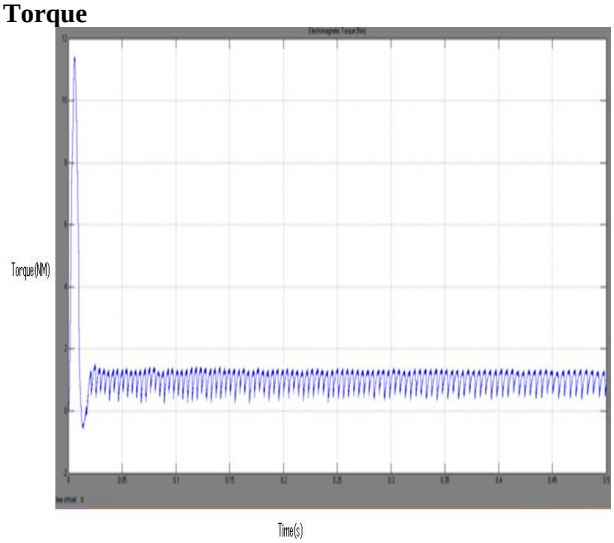

Fig.16 Torque waveform of BLDC motor

Inference from Simulation Results

Conventional Drive system

Fig.8 shows the stator current is less than the rated current 1A. Fig.9 shows wide range of variation in the speed. Fig.10 shows that the torque obtained is less than the rated torque 1.4 Nm

SEPIC

Fig.11 shows that the Current value exceeds the rated current (1A) and shoots up to 6A. Fig.12 shows that the Speed shoots up to 3500 rpm. Fig.13 shows the torque increases beyond rated torque.

CSC

Fig.14 shows the Stator current waveform has less distortion and rated current 1A is obtained. Fig.15 shows wide range of speed control is achieved. Fig.16 shows Torque waveform has less ripples and rated torque 1.4 Nm is obtained.

Comparison of Simulation Results for Various Converter Topologies

Table 1. Simulation Results

Performances Indices	Conventional system	CSC converter	SEPIC
PF	0.7419	0.8501	0.1296
THD	0.4507	0.2996	0.5407

From the simulation circuit PF and THD are measured and the results obtained are tabulated respectively for conventional converter based drive system, CSC converter based drive and SEPIC based drive system. From the results it is proved that the proposed drive system provides reduced THD and improved PF.

Conclusion

This paper deals with the analysis and implementation of efficient BLDC drive with different converter topologies. Performance analysis is carried out using Matlab simulation circuit respectively for Conventional, SEPIC and CSC based drive systems. From the simulation results obtained it is proved that the proposed CSC converter fed drive system provides better performance by considering PF and THD compare to conventional and SEPIC system. A single stage PFC based CSC converter system has been designed and validated for the speed control with improved power quality at the AC mains for a wide range of speed. The proposed drive system has been found suitable among various adjustable speed drives for many low power applications

Appendix

PMBLDC Motor Rating: 4 pole, Prated (Rated Power) = 220 W, T rated (Rated Torque) = 1.4 Nm, Kb (Back EMF Constant) = 146.6077 V/krpm, Kt (Torque Constant) = 0.49 Nm/A, R ph (Phase Resistance) = 2.8 Ω, L (Phase Inductance) = 8.5 mH.

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